CLAIMS

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1. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate adjacent to said P well;

an N type active region defined in said P well;

a P type active region defined in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region; and

a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

2. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film

comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

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a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

3. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polycilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer.

4. A memory cell comprising:

a semiconductor substrate;

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a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said diffusion barrier layer does not extend over a substantial portion of said N+ polysilicon layer.

5. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

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a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines an N type common boundary with said N+ polysilicon layer that is significantly larger than a P type common boundary defined by said metal, metal silicide, or metal nitride film and said P+ polysilicon layer.

6. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polycilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer.

7. A memory cell comprising:

a semiconductor substrate;

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a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said diffusion barrier layer does not extend over a substantial portion of said P+ polysilicon layer.

8. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

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a diffusion barrier layer formed in said polycilicide gate electrode structure over a substantial portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines a P type common boundary with said P+ polysilicon layer that is significantly larger than an N type common boundary defined by said metal, metal silicide, or metal nitride film and said N+ polysilicon layer.

9. A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure over said N+ polysilicon layer and said P+ polysilicon layer between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polycilicide gate electrode structure and said diffusion barrier layer are arranged such that

migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer and

migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer.

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10. An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

11. An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

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a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film having a thickness of between about 500 Å and about 4000 Å and an overlying metal, metal silicide, or metal nitride film having a thickness of between about 500 Å and 4000 Å, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer having a thickness of between about 10 Å and about 15 Å formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

12. An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said N+ polysilicon layer and said P+ polysilicon layer.

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13. An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polycilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer.

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14. An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polycilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said diffusion barrier layer.

15. A memory cell array comprising a plurality of SRAM cells arranged in rows and columns, wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

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a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

16. A computer system including a microprocessor in communication with a memory cell array via a data communication path, wherein said memory cell array comprises a plurality of SRAM cells arranged in rows and columns, and wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

a diffusion barrier layer formed in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

~~17. A method of fabricating an SRAM memory cell, said method comprising:~~

~~providing a semiconductor substrate;~~

~~forming a P well in said semiconductor substrate;~~

~~forming an N well in said semiconductor substrate;~~

~~providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;~~

~~arranging an isolation region to isolate said N type active region from said P type active region;~~

~~providing a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and~~

~~forming a diffusion barrier layer in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.~~

18. A method of fabricating an SRAM memory cell, said method comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a P type active region of a pull-up transistor in said N well;

forming a gate oxide layer and a conductive gate of said pull-up transistor over said P type active region;

forming an N type active region of a pull-down transistor in said P well;

forming a gate oxide layer and a conductive gate of said pull-down transistor over said N type active region;

forming an isolation region between said N type active region and said P type active region;

forming a polycrystalline silicon film over said pull-down transistor and said pull-up transistor;

doping selectively said polycrystalline silicon film to form an N+ polysilicon layer over said pull-down transistor and a P+ polysilicon layer over said pull-up transistor;

forming a diffusion barrier layer over a substantial portion of said polycrystalline silicon film; and

forming a metal, metal silicide, or metal nitride film over said doped polycrystalline silicon film and said diffusion barrier layer.

19. A method of fabricating a memory cell array by arranging a plurality of said SRAM cells in rows and columns and connecting each SRAM cell of said array to a word line and to a pair of bit lines, wherein each of said SRAM cells is fabricated by:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

arranging an isolation region to isolate said N type active region from said P type active region;

providing a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming a diffusion barrier layer in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

20. A method of fabricating a computer system by arranging a microprocessor in communication with a memory cell array via a data communication path and fabricating said memory cell array by arranging a plurality of said SRAM cells in rows and columns and connecting each SRAM cell of said array to a word line and to a pair of bit lines, wherein each of said SRAM cells is fabricated by:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

arranging an isolation region to isolate said N type active region from said P type active region;

providing a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming a diffusion barrier layer in said polycilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

21. A memory cell as claimed in claim 2 wherein said diffusion barrier layer comprises an ultrathin diffusion barrier layer.

22. A memory cell as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of less than 125 Å.

23. A memory cell as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 10 Å and about 15 Å.

24. A memory cell as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 125 Å.

25. A memory cell as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 50 Å.

26. A memory cell as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 125 Å and said polycrystalline silicon film has a thickness of between about 500 Å and about 4000 Å.

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27. A memory cell as claimed in claim 5 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said P+ polysilicon layer and wherein said diffusion barrier layer is formed in said polycilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said P+ polysilicon layer over the entire extent of said overcoated portion of said P+ polysilicon layer.

28. A memory cell as claimed in claim 8 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said N+ polysilicon layer and wherein said diffusion barrier layer is formed in said polycilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said N+ polysilicon layer over the entire extent of said overcoated portion of said N+ polysilicon layer.

29. A method of fabricating an SRAM memory cell as claimed in claim 18 wherein said diffusion barrier layer is formed by selective chemical oxidation of said polycrystalline silicon film.

30. A method of fabricating an SRAM memory cell as claimed in claim 18 wherein said diffusion barrier layer is formed by silicon nitride deposition.

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